

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KENNETH C. CURT, EDWARD J. CHEJLAVA JR.,
and ANTHONY KOZACZUK

Appeal No. 97-1213
Application No. 08/459,561¹

ON BRIEF

Before THOMAS, KRASS, and SMITH, Administrative Patent Judges.
KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 51 and 52. Claim 53 has been allowed by the examiner.

¹ Application for patent filed June 2, 1995. According to appellants, this application is a divisional of Application 08/356,926, filed December 14, 1994, now abandoned; which is a continuation of Application 07/964,590, filed October 20, 1992, now abandoned.

The invention pertains to a method for transferring data between a computer bus and a peripheral bus using an interface device, the nature of which is apparent from a review of independent claim 51 reproduced as follows:

51. A method for transferring data between a computer bus and a peripheral bus using an interface device coupled between said computer bus and said peripheral bus, said method comprising the steps of:

receiving from said computer a request for an nth datum;

reading and storing into said interface device said nth datum from said peripheral bus; and

reading and storing into said interface device an n+1th datum from said peripheral bus before said computer bus transmits a request for said n+1th datum, said n+1th datum having an address adjacent to an address of said nth datum read from said peripheral bus.

The examiner relies on the following reference:

Barrett et al. [Barrett]	5,136,692	Aug.
4, 1992		

Claims 51 and 52 stand rejected under 35 U.S.C. § 103 as unpatentable over Barrett.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

We affirm.

As the examiner appears to read Barrett on claim 51, Barrett's adapter 14 is analogous to the claimed "interface device" and bus 12 is the claimed "computer bus." It is clear that adapter 14 receives from the computer bus 12 a request for an nth datum which is then retrieved from a disk via a peripheral bus and the nth datum is read and stored into the adapter (adapter cache 54).

Barrett also provides for "read ahead" commands wherein a device driver within the processor 30 "provides a read ahead command that is an anticipatory command anticipating the future read command for a certain block of data" [column 3, lines 63-66]. These read ahead commands for the n+1th datum cause a reading and storing into the adapter 14 from the peripheral bus. The issue before us, and as argued by appellants, is whether this reading and storing of the n+1th datum is "before said computer bus transmits a request for said n+1th datum," as claimed.

Appellants argue that Barrett does not teach or suggest this claimed limitation because the read ahead command is provided by the device driver in Barrett which is located within processor 30. Therefore, reason appellants, the read

ahead commands must pass over the computer bus 12 (from processor 30 to adapter 14) which is contrary to the requirement of claim 51 that the read ahead of the n+1th datum must be "before the computer bus transmits a request for the n+1th datum." We might agree with appellants' position if the cited claim language read "before said computer bus transmits any request for said n+1th datum." However, as presently written, it is our view that the instant claim language is broad enough to cover the situation disclosed by Barrett.

The instant claim language does not preclude an original read ahead command being issued by the device driver over computer bus 12 to the adapter 14 in Barrett. The adapter 14 then retrieves the n+1th datum from a disk and places it in the adapter cache. It may never be used but the system awaits a formal request by the processor 30 for the n+1th datum. Should that formal request for the n+1th datum come from processor 30, i.e., the computer bus transmits a request for said n+1th datum, the n+1th datum has already been read and stored into the adapter 14 ("said interface device") by the previous read ahead command and it has been done "before said computer bus transmits a request for said n+1th datum," as

required by the claim. Again, had the claim required "before the computer bus transmits any request for said n+1th datum," this would have precluded the first read ahead command from the device driver since that command would have had to be transmitted by the computer bus.

Thus, we do not read claim 51 as precluding the situation wherein the anticipatory read ahead command from the device driver over the computer bus causes the n+1th datum from being stored in the adapter cache and, when, and if, the actual command comes from the computer to read the n+1th data, it can be reasonably said that the n+1th datum has been read and stored from the peripheral bus into the interface (adapter) device "before said computer bus transmits a request [i.e., the actual request, as opposed to the read ahead request] for said n+1th datum..."

Claim 52 falls with claim 51 as there is no separate argument by appellant as to the merits of the additional limitation of claim 52.

The examiner's decision rejecting claims 51 and 52 under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in
connection with this appeal may be extended under 37 CFR
§ 1.136(a).

AFFIRMED

JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
ERROL A. KRASS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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